

FIG. 1

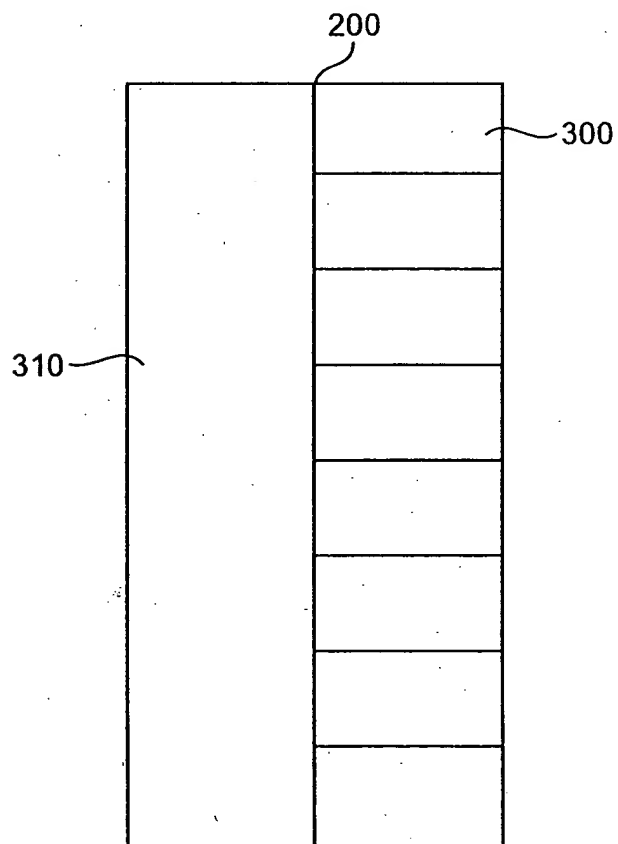
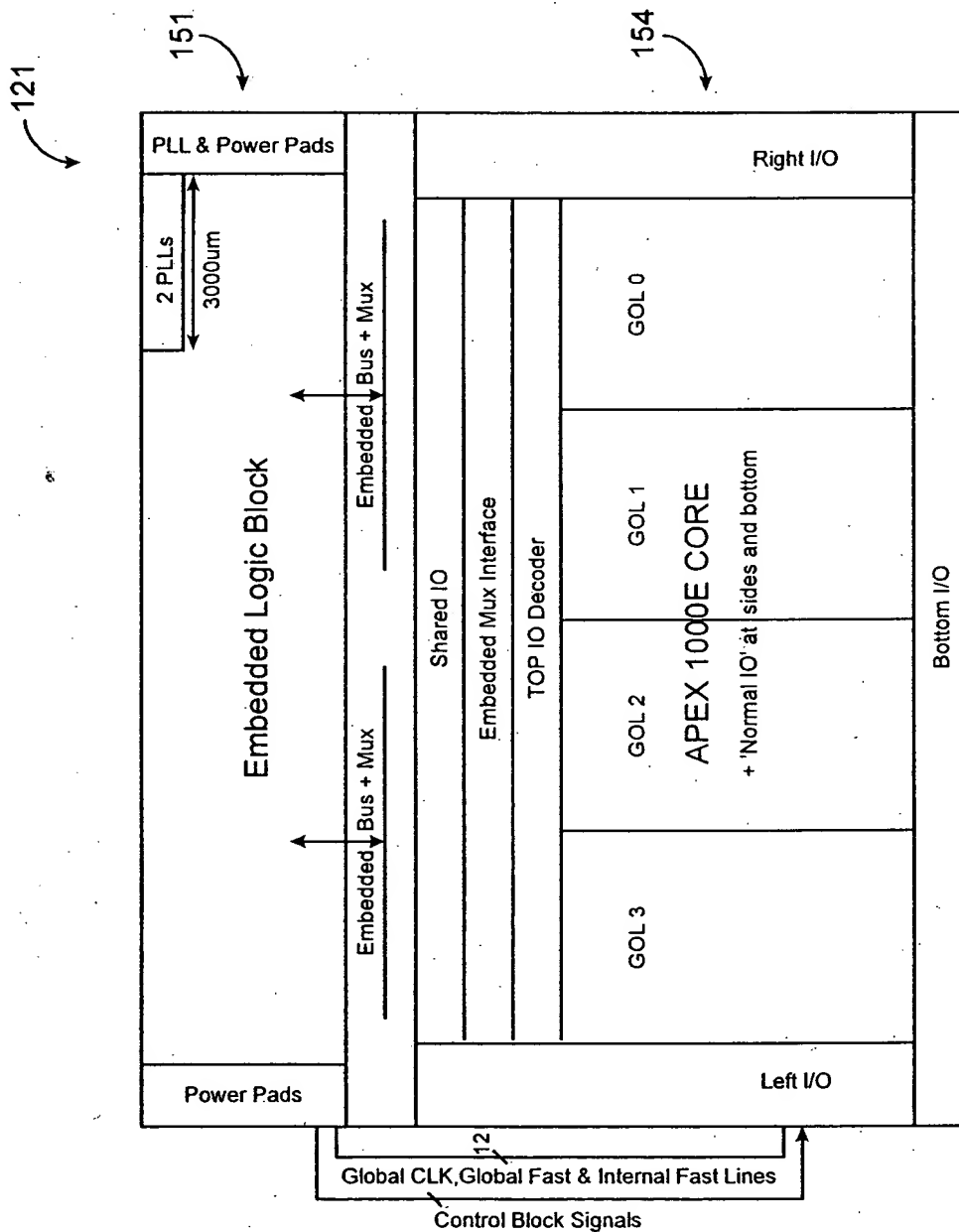


FIG. 4



Top Level Floor Plan

FIG. 2

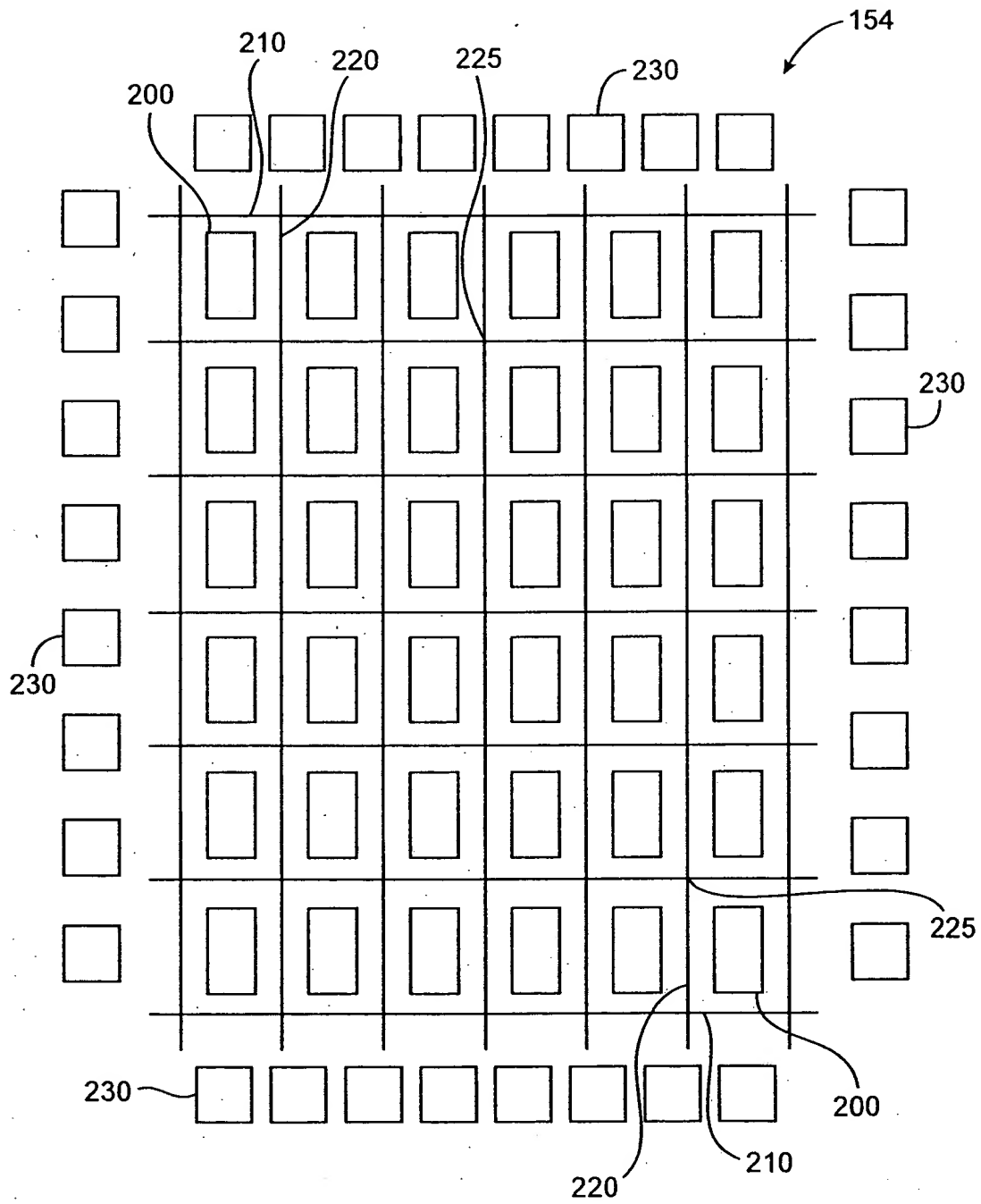


FIG. 3



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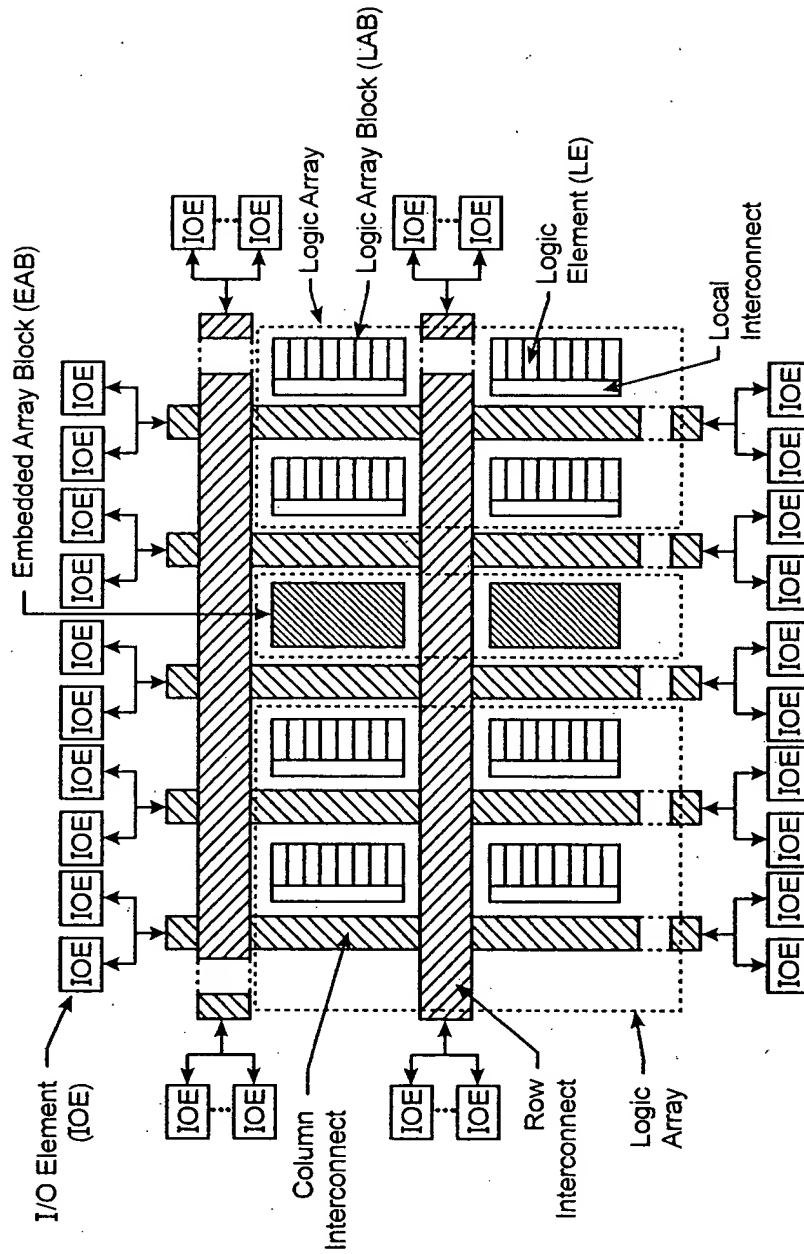


FIG. 5

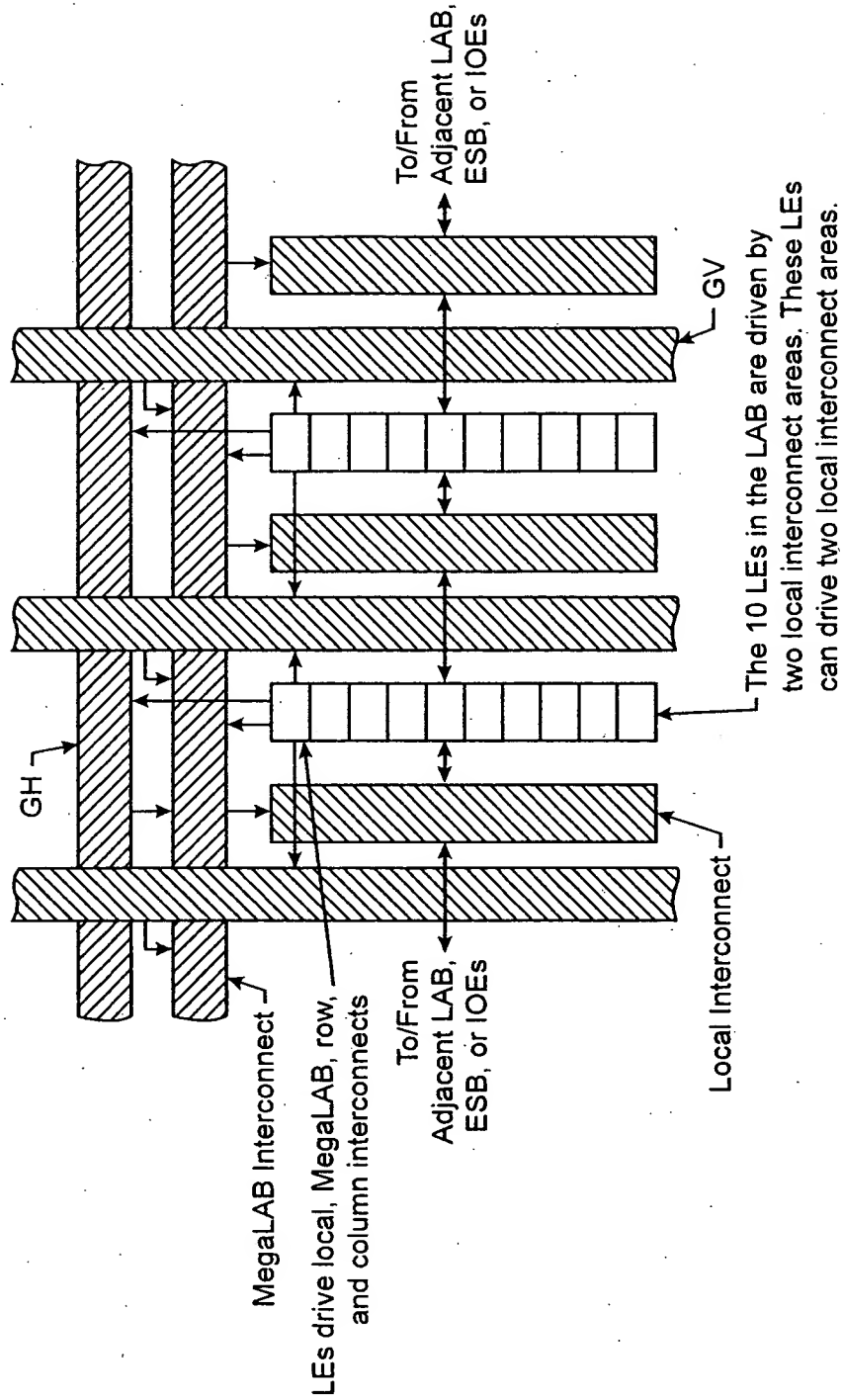


FIG. 6

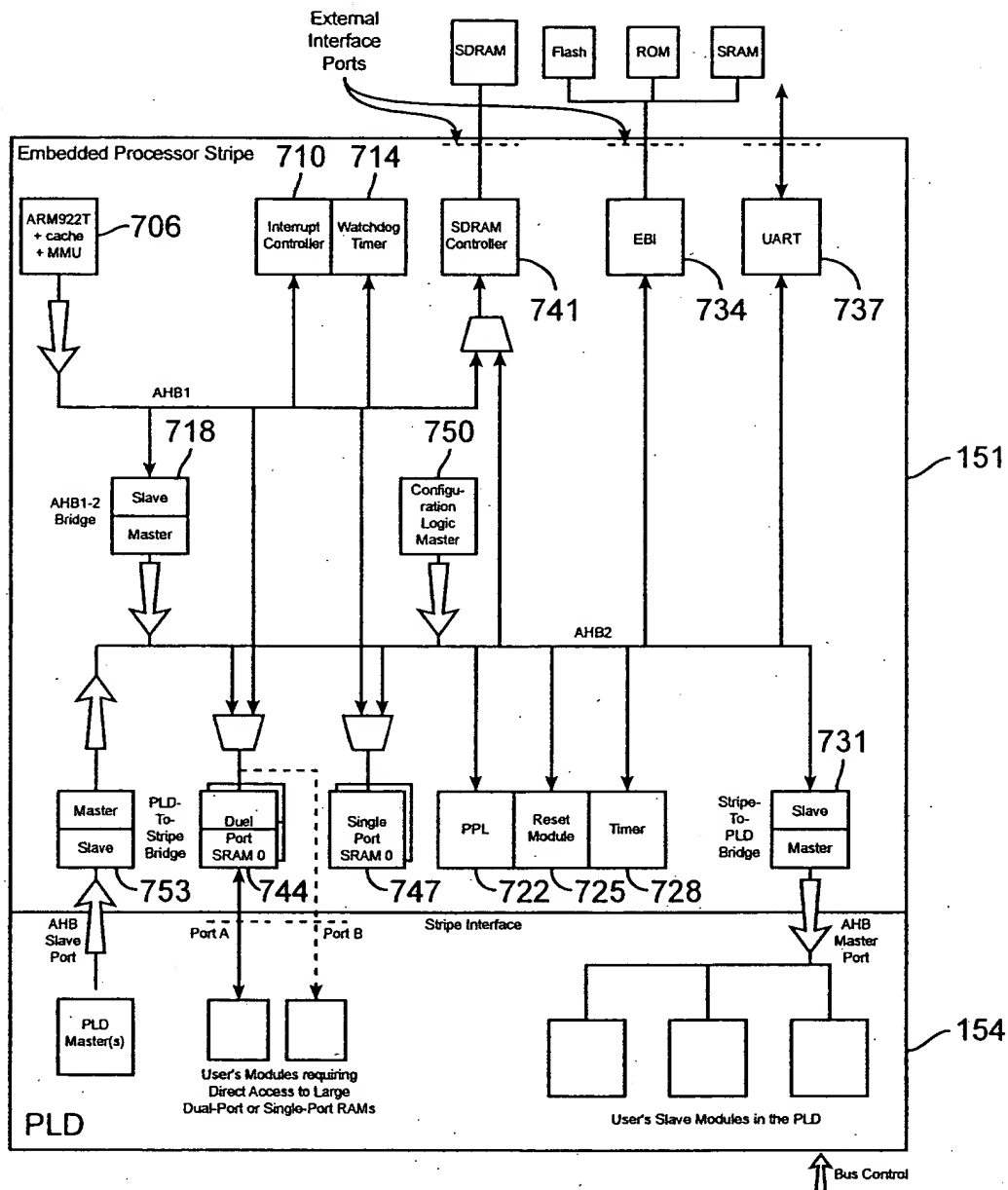


FIG. 7



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FIG. 8

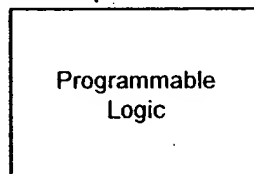


FIG. 9

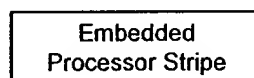
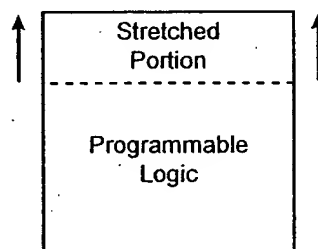
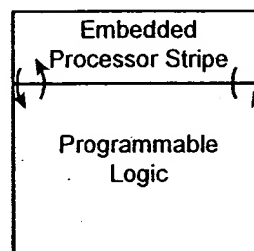


FIG. 10



Embedded Processor Stripe

FIG. 11



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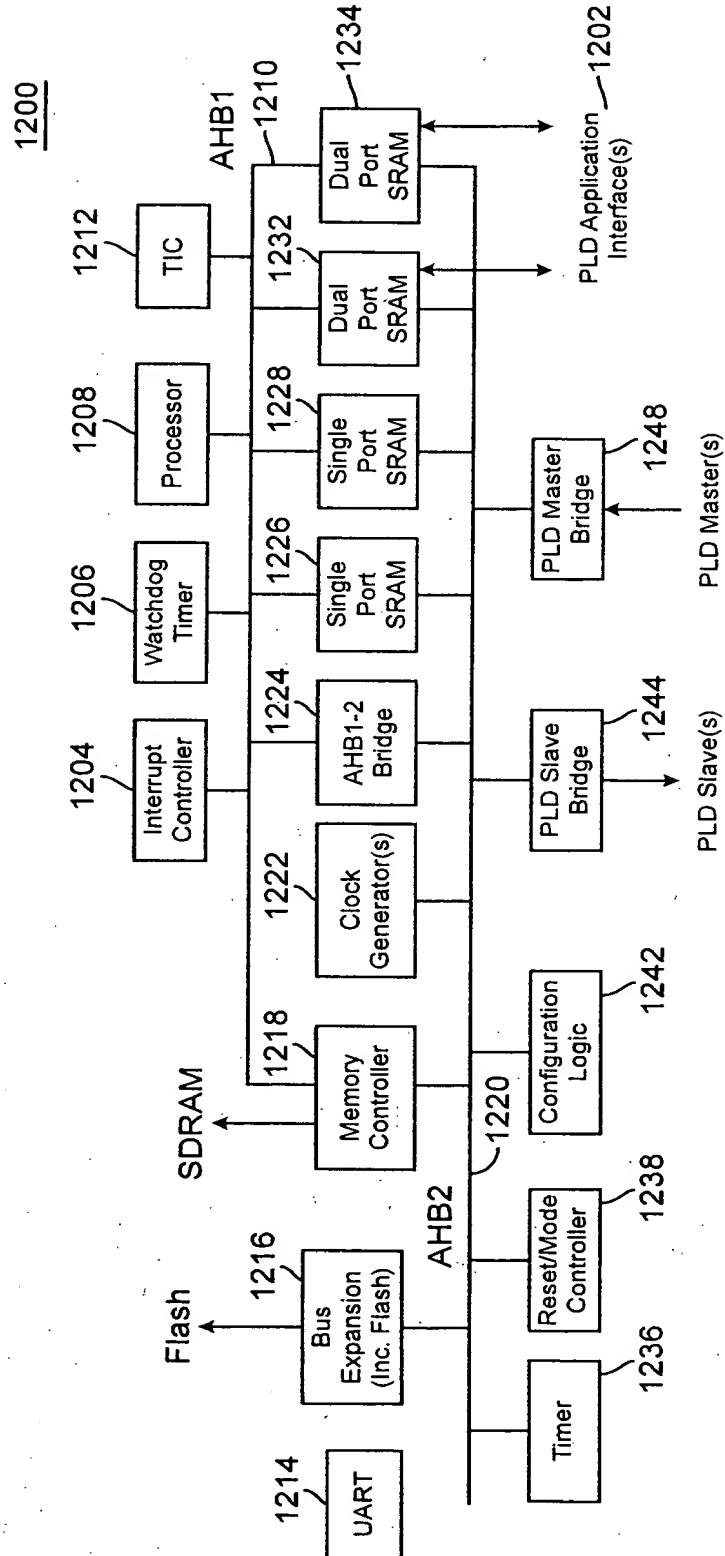


FIG. 12





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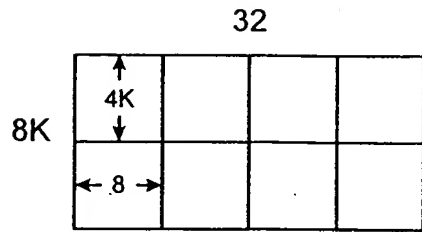


FIG. 13A

8K X 32

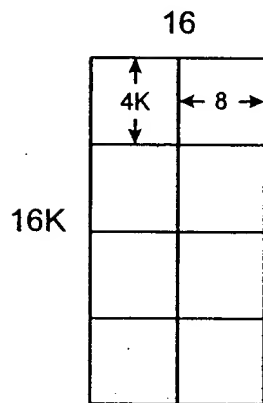


FIG. 13B

16K X 16

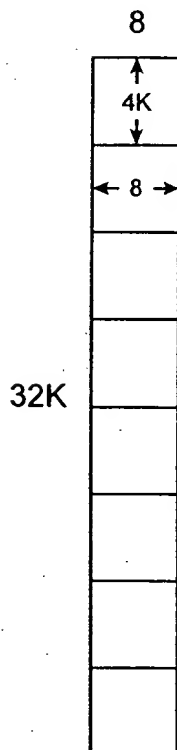


FIG. 13C

32K X 8

+



+

1400

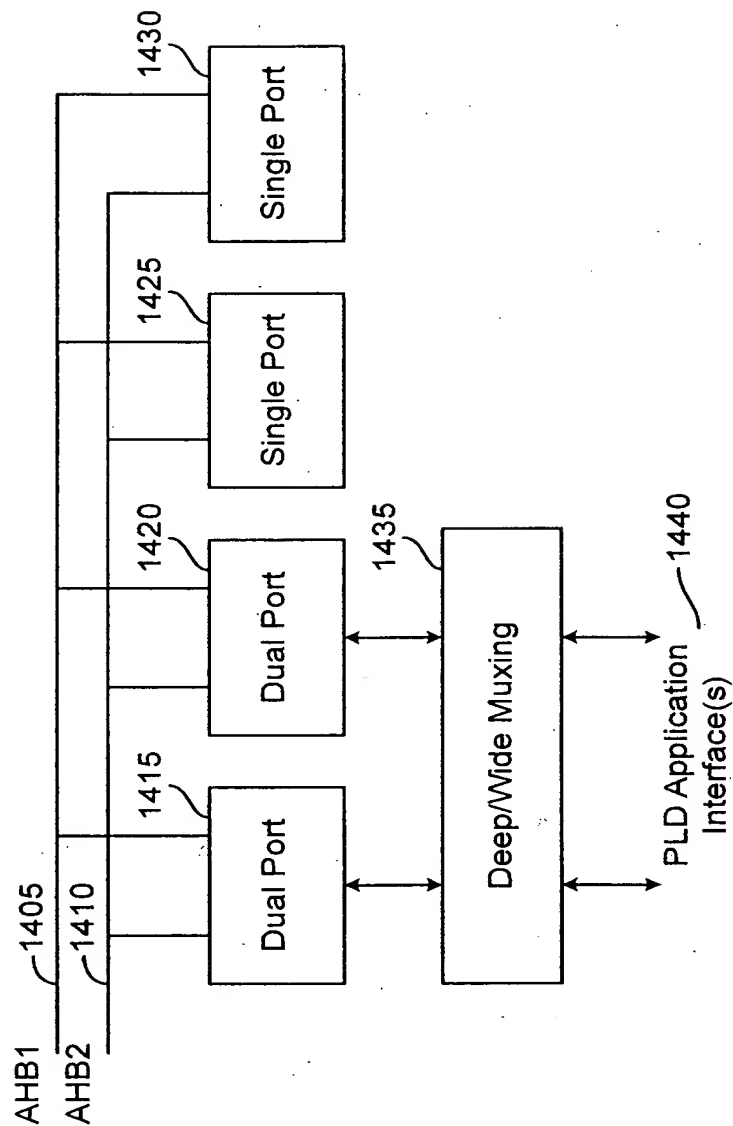


FIG. 14

+

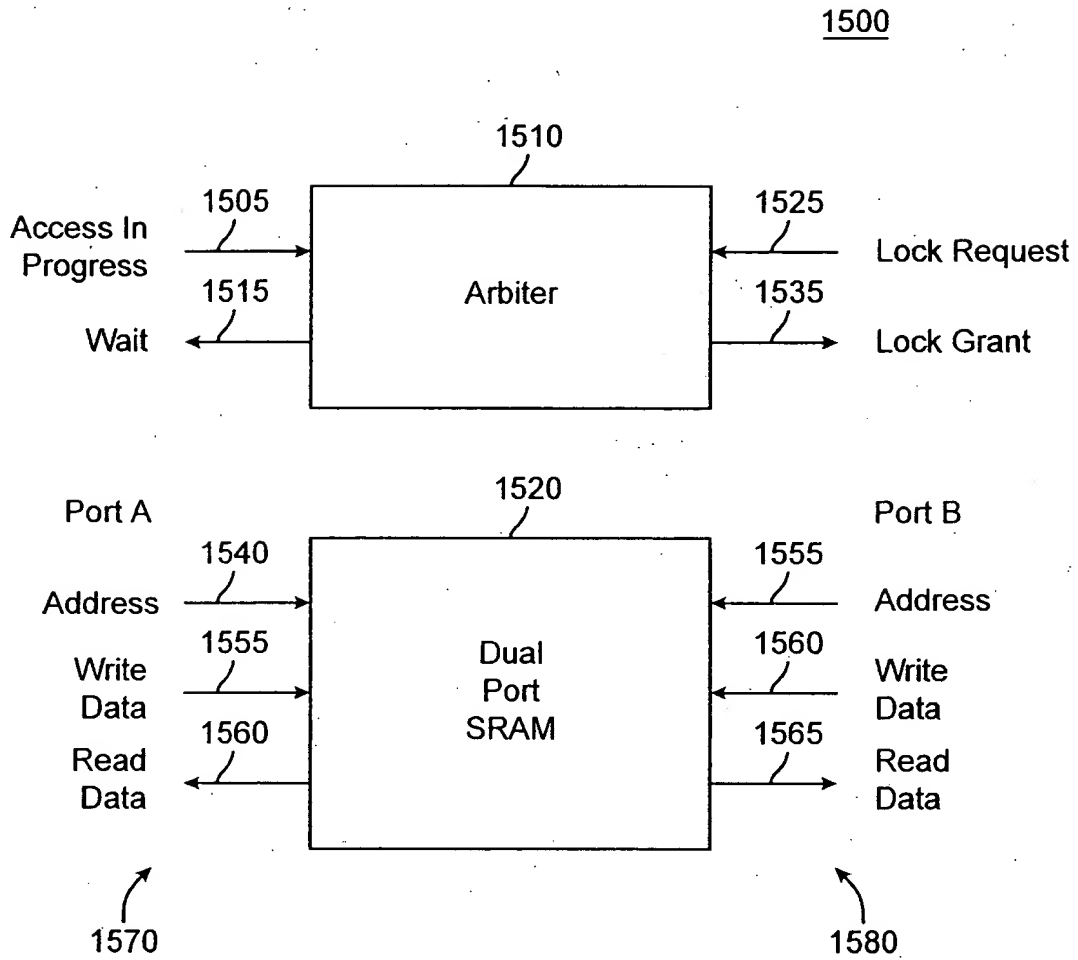


FIG. 15

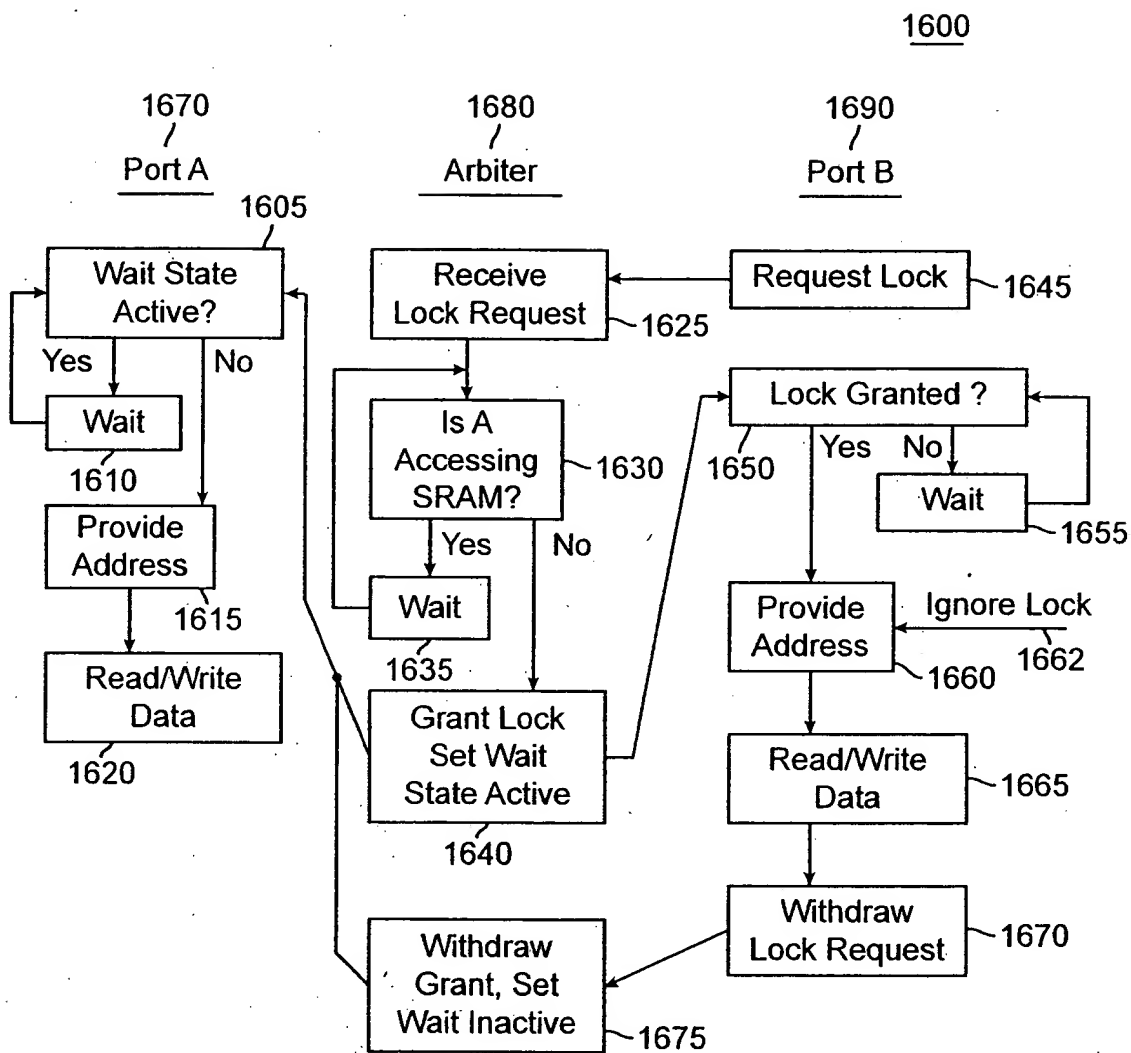


FIG. 16

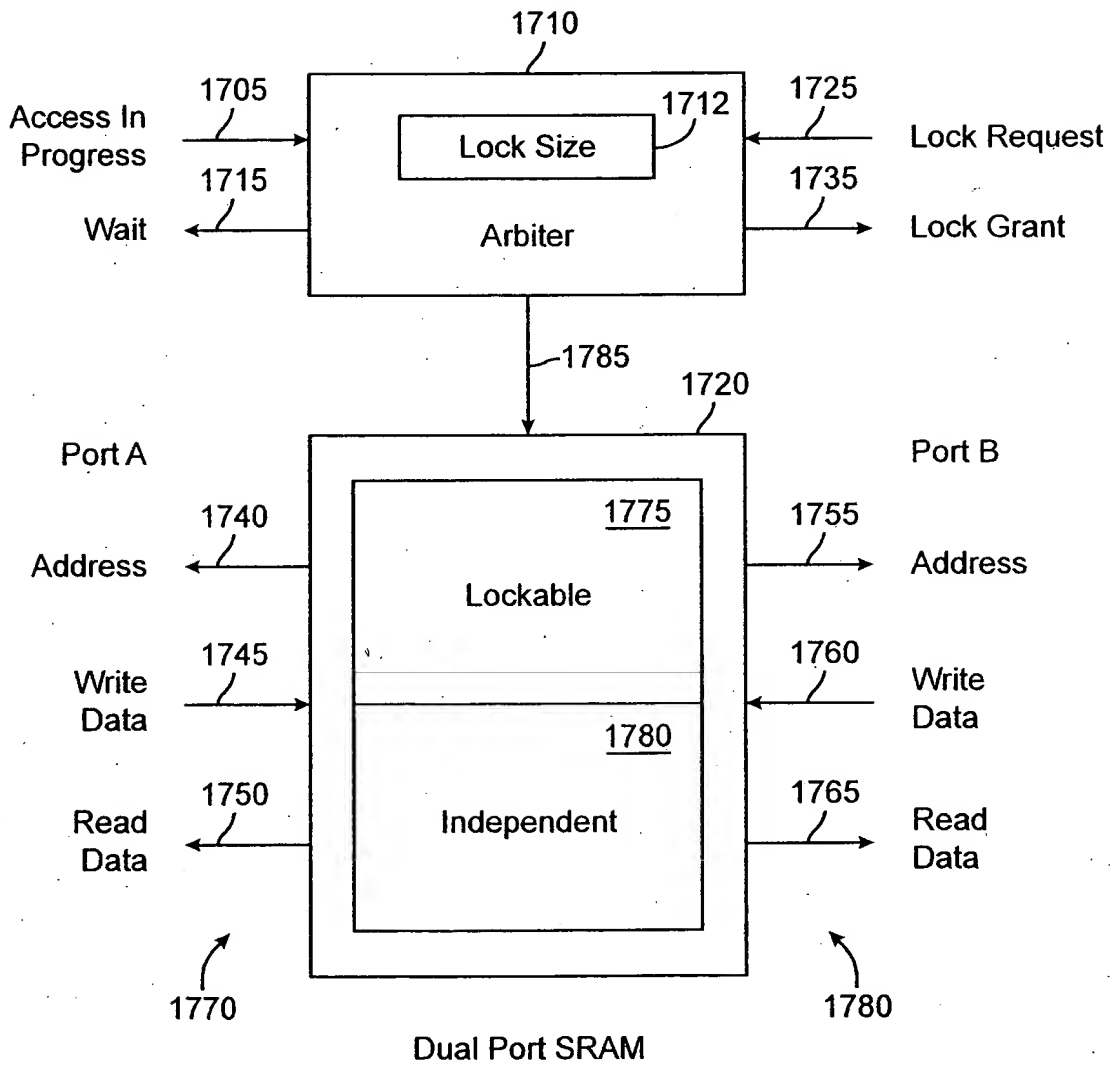


FIG. 17

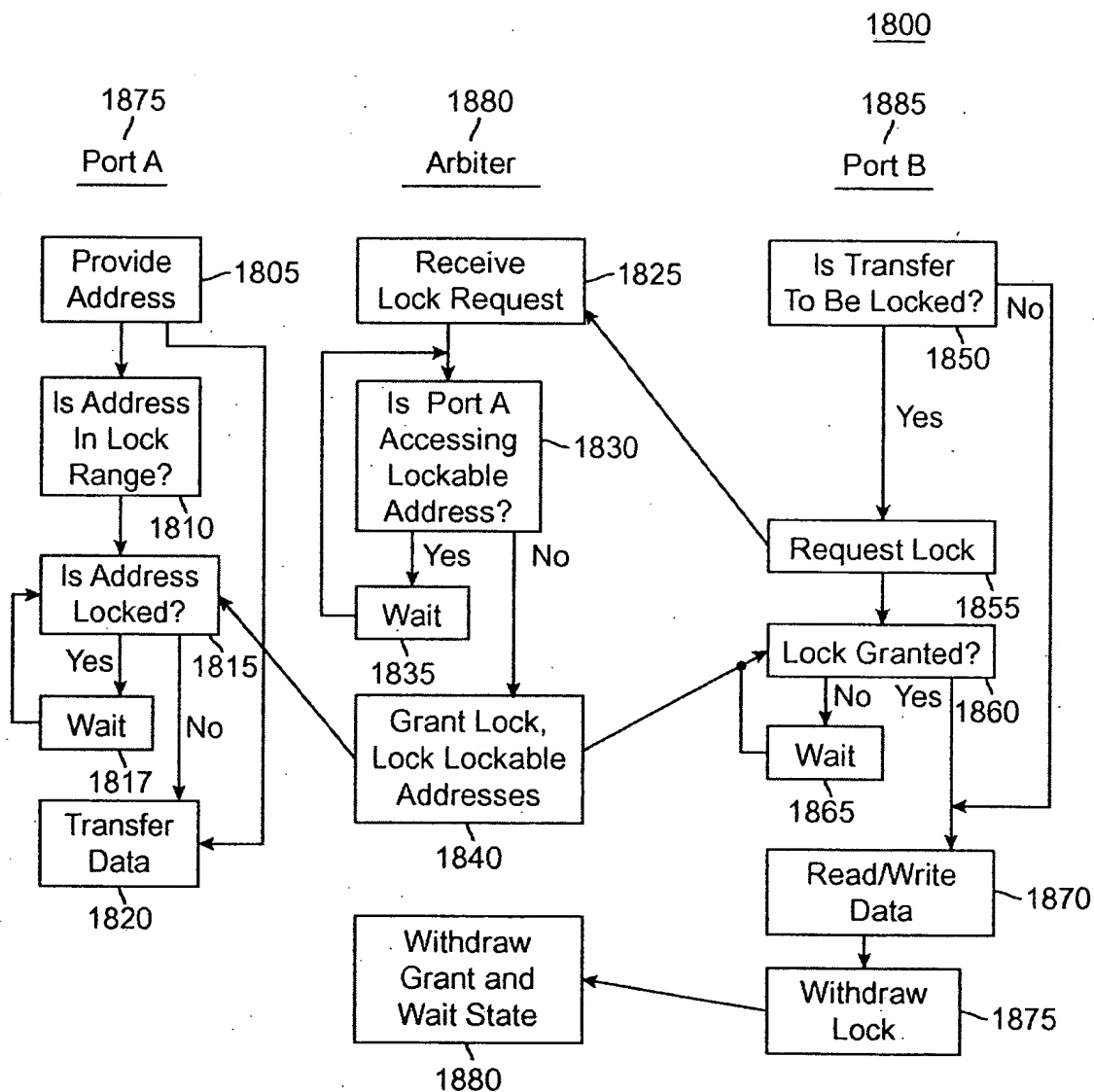


FIG. 18

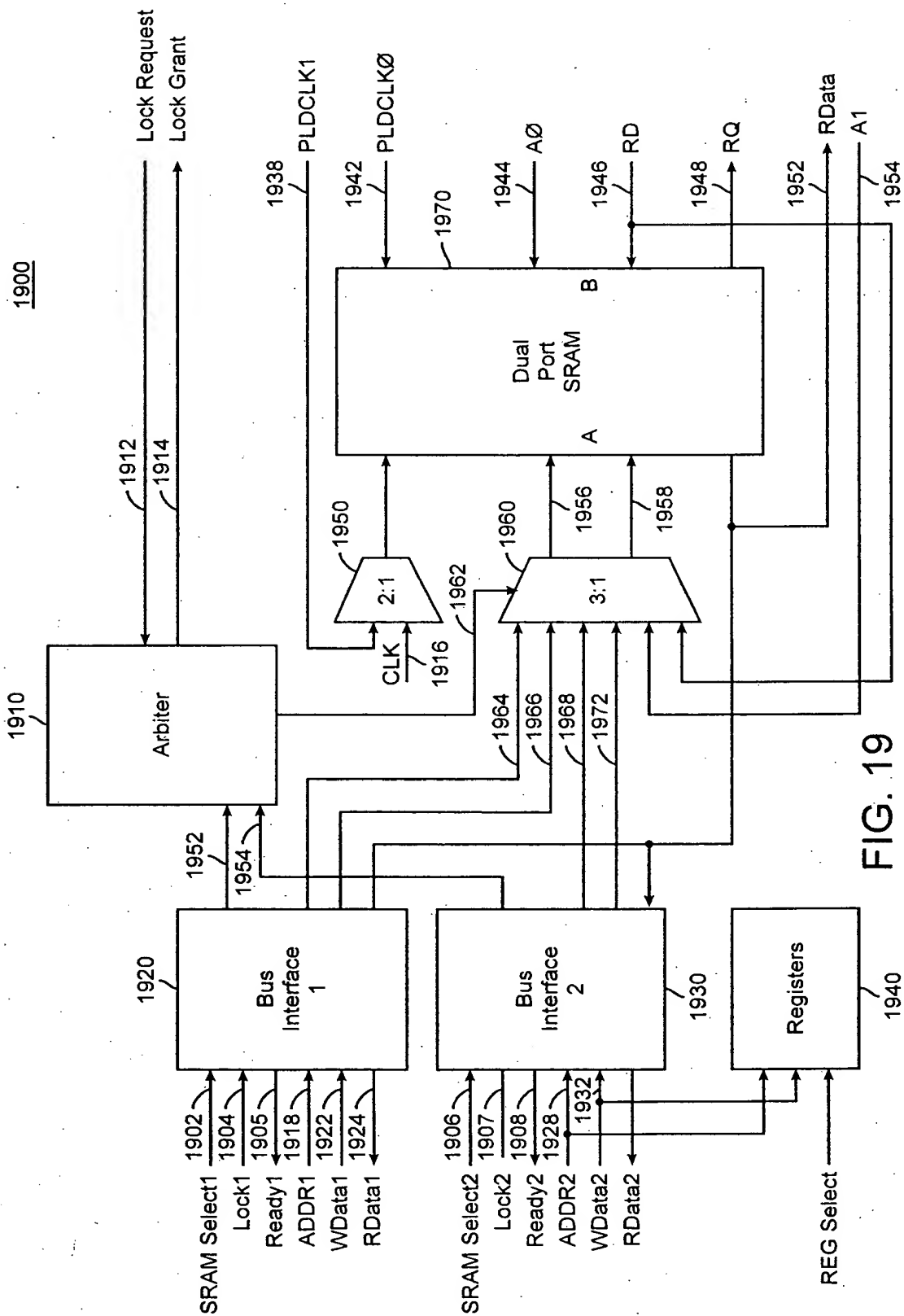
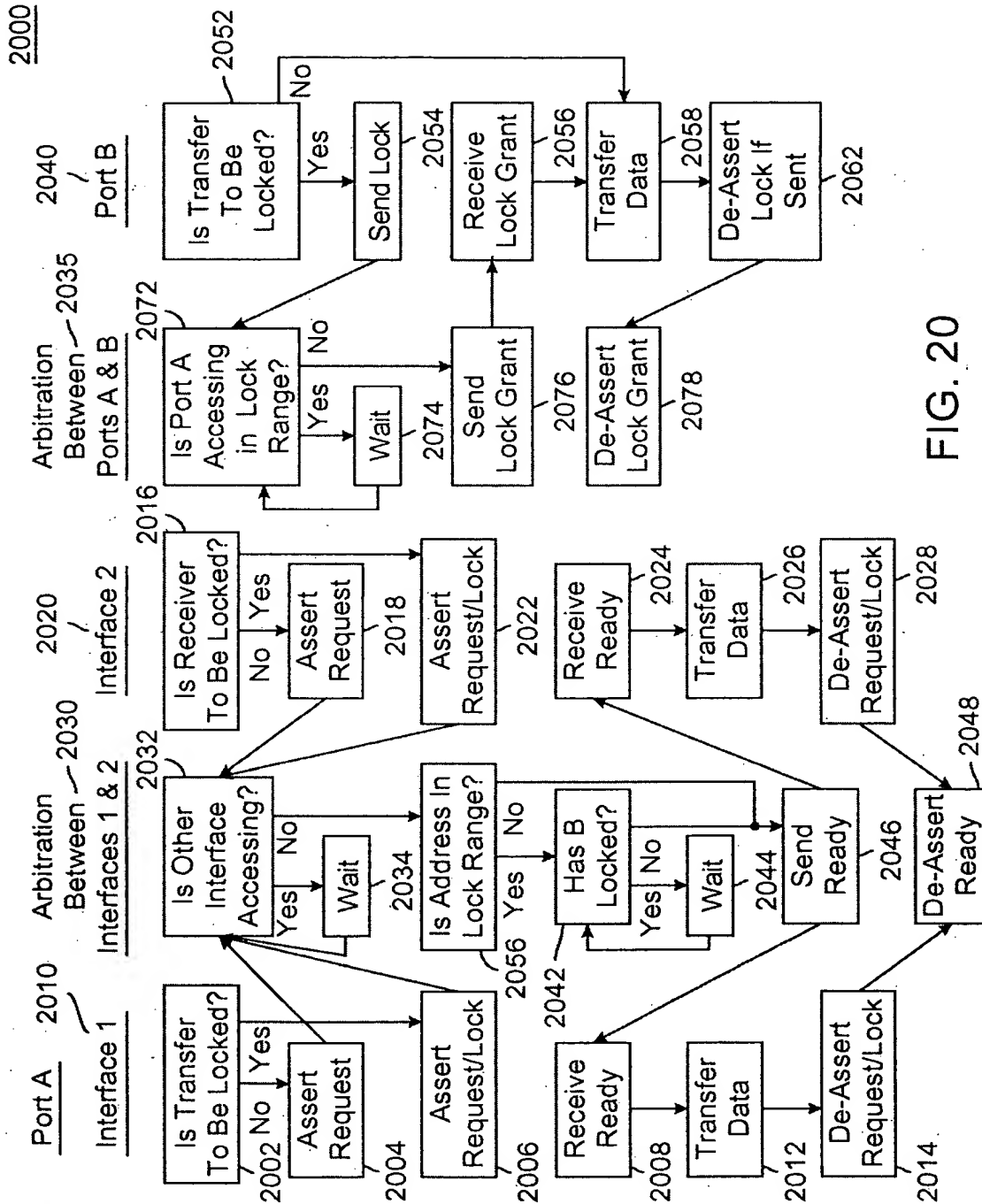


FIG. 19





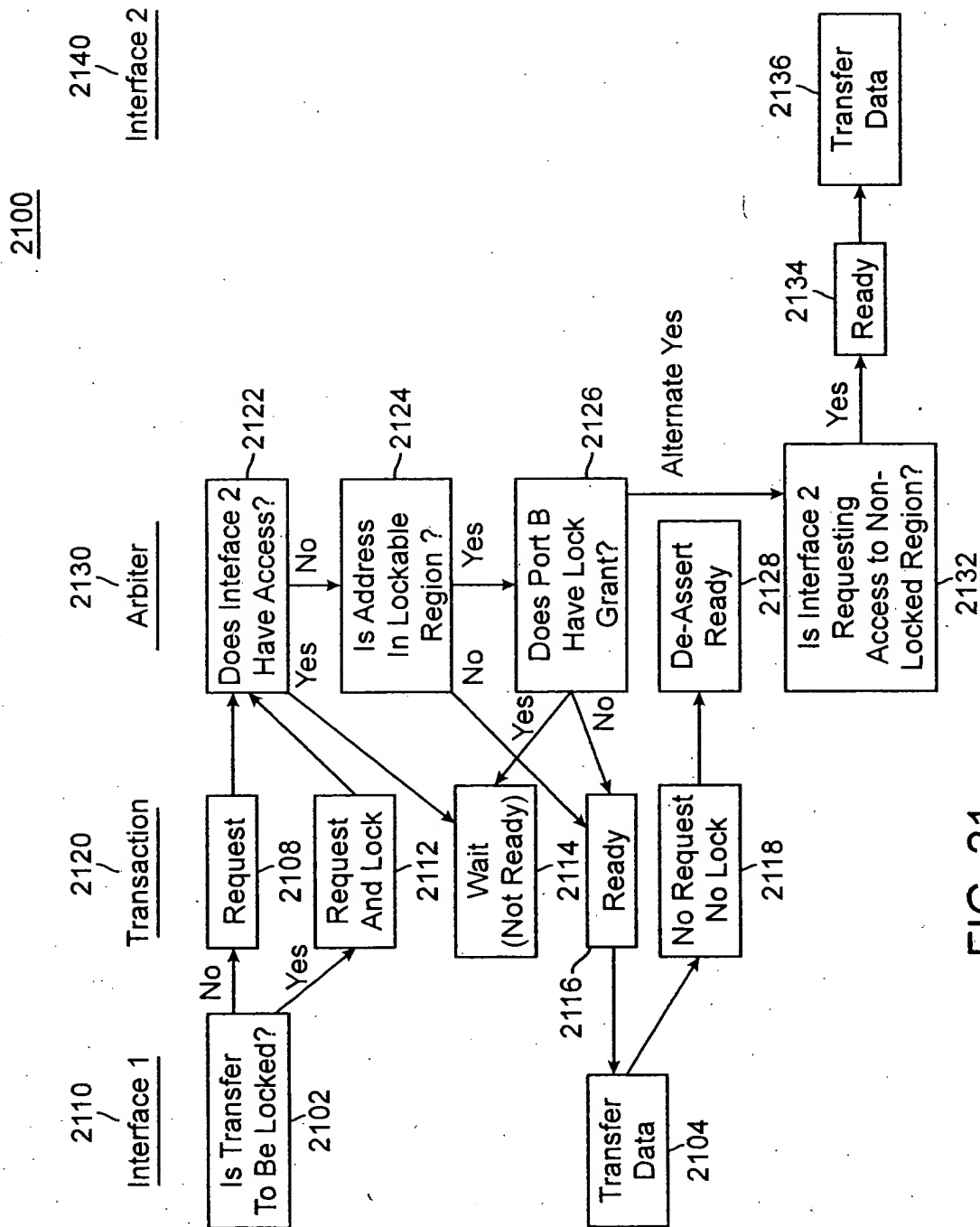


FIG. 21

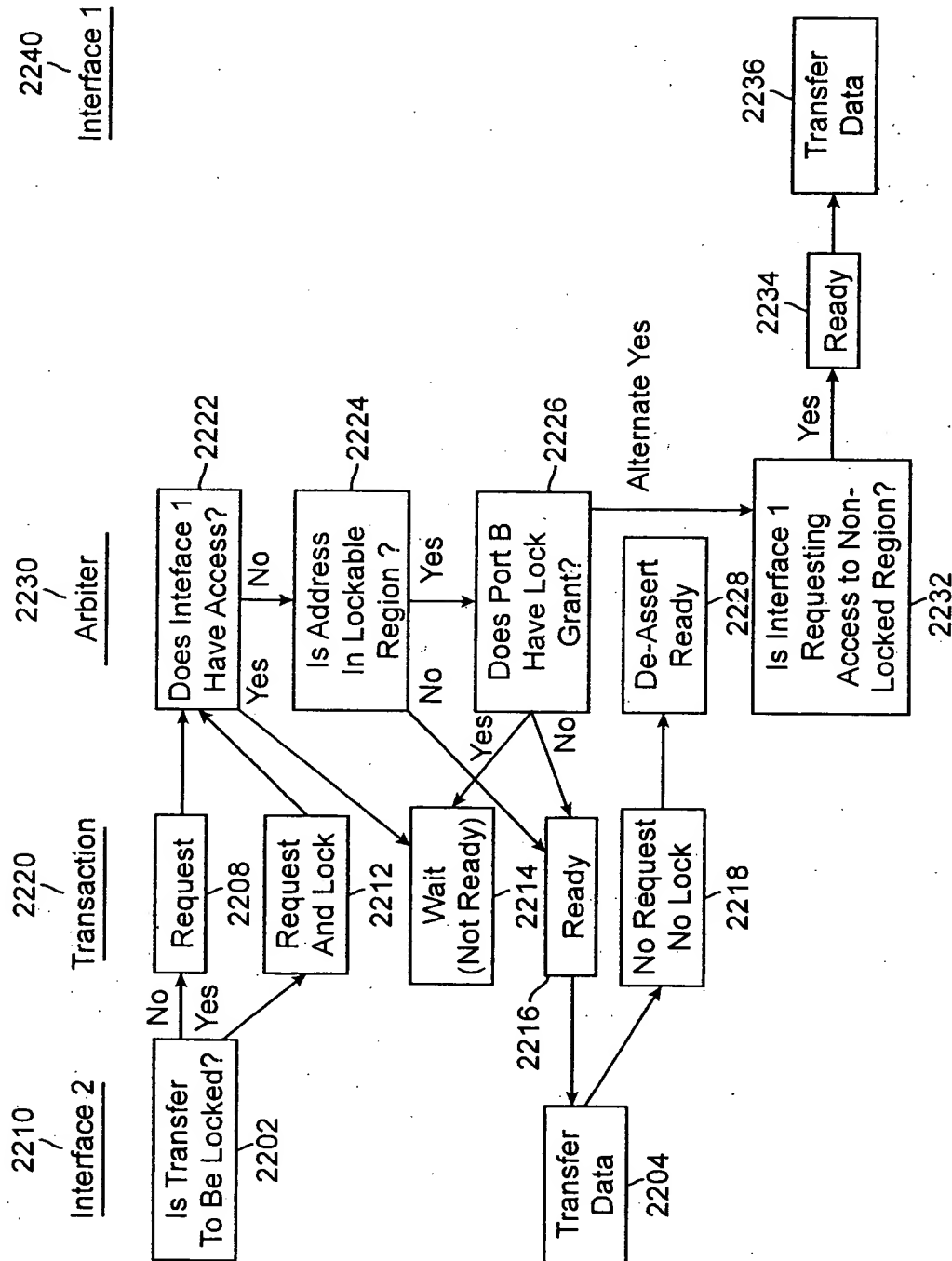


FIG. 22

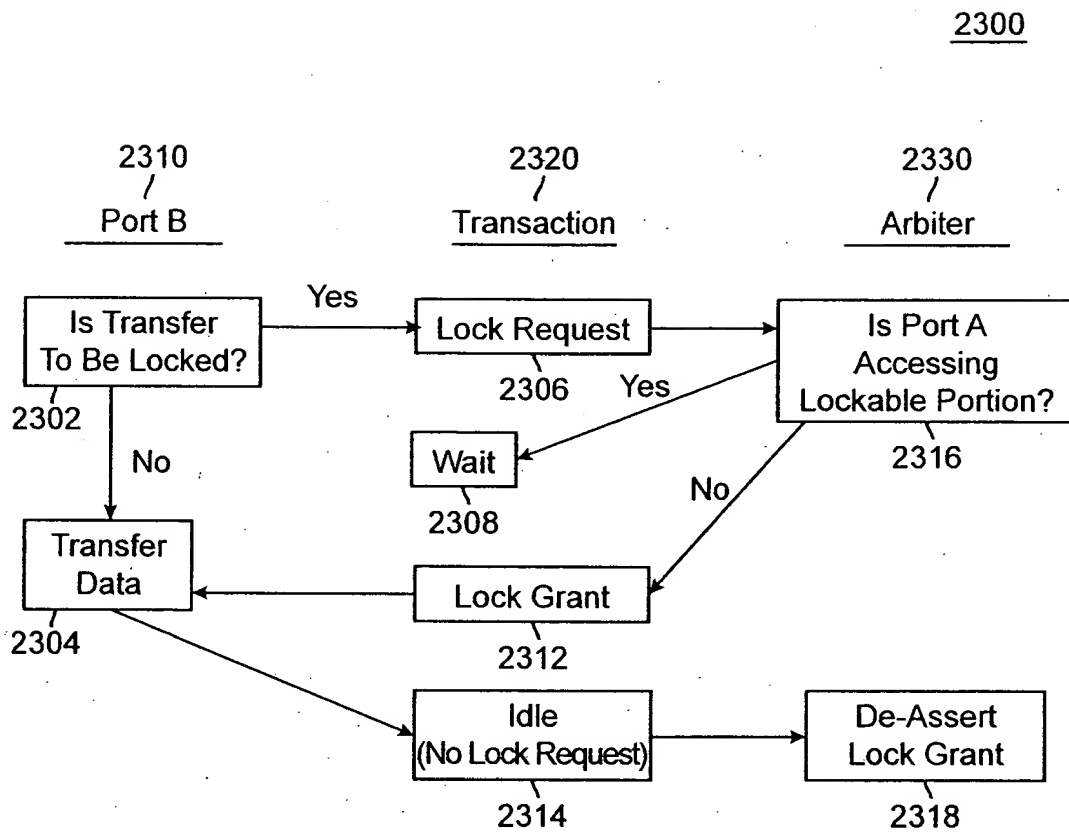


FIG. 23

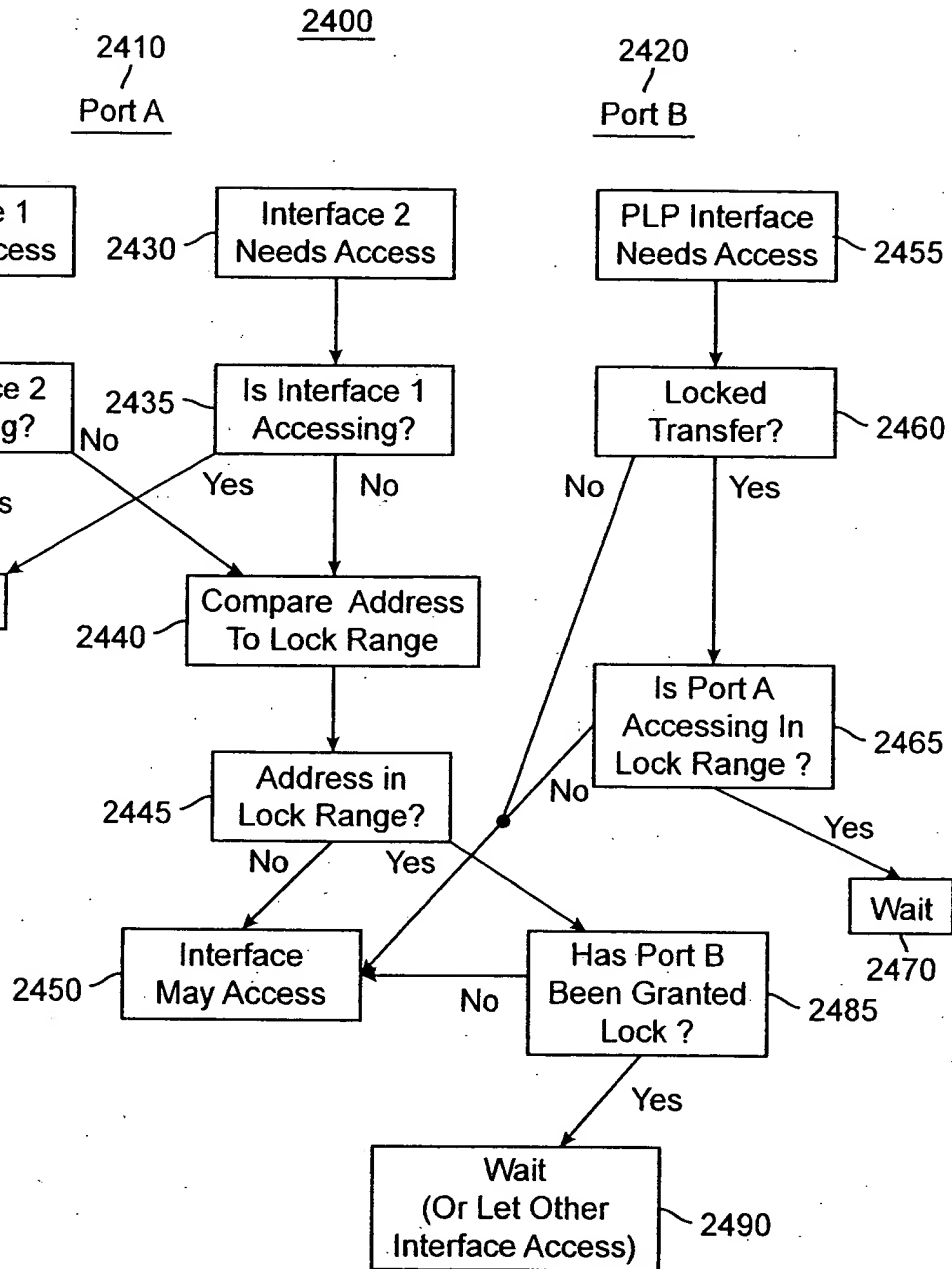


FIG. 24

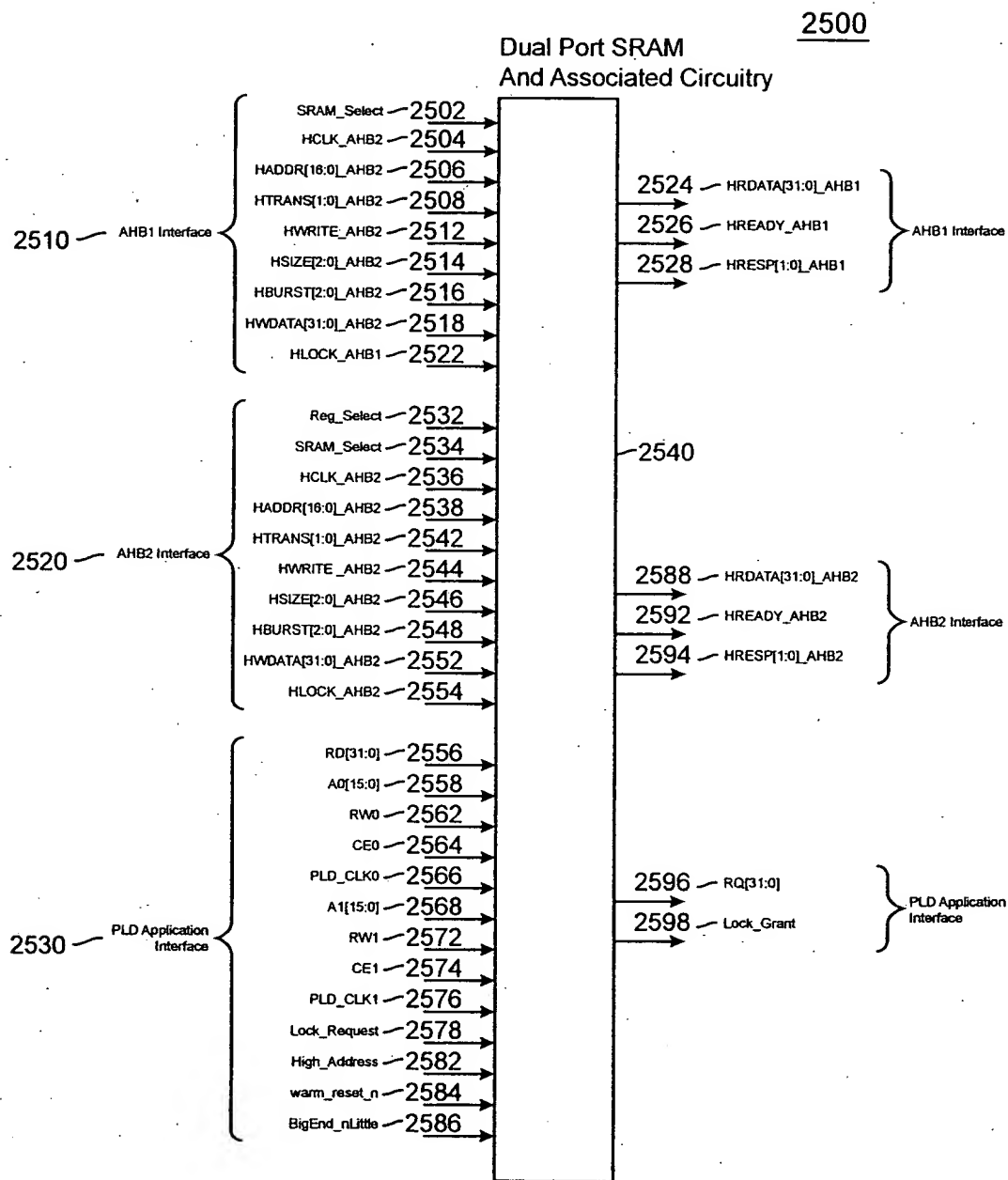


FIG. 25